Solid State Devices: Assignments for Lectures 19-42

Lec 19: P-N Junction – Structure and characteristics to be modeled

1) Sketch the following for a small-signal p-n junction *to scale*: (a) cross-section and top view of the device structure; (b) DC current-voltage curve at two different temperatures.

Lec 20, 21: P-N Junction under equilibrium

2) Based on energy bands or otherwise, explain whether the built-in voltage of a p-n junction decreases or increases with temperature.

3) Sketch the energy band diagram for an n-n^+ junction in silicon under equilibrium.

4) Sketch the distributions of n, p, ρ, E and ψ for an n-n^+ junction in silicon under equilibrium.

Lec 22, 23: P-N Junction under forward bias

5) Determine the pn product as a function of distance in the space-charge region of a p-n junction under applied bias.

6) An abrupt Silicon p-n junction has a junction area of 10^{-2} cm^{-2} and operates at 300 K. The p-side has N_a = 1 x 10^{17} cm^{-3} and $\tau_n = 10^{-7}$ s, and the n-side has N_d = 1 x 10^{16} cm^{-3} and $\tau_p = 10^{-6}$ s. (a) Calculate the depletion width on either side of the junction. (b) Calculate the maximum forward bias and the corresponding current for which the low-level injection approximation in the lightly doped region remains valid. (c) Calculate the location of the plane with reference to the depletion edge at which the majority and minority carrier currents are equal in magnitude for this forward bias.

7) Assume that all approximations of the ideal diode model apply, and that the lifetime in the n and p regions is the same. Establish the validity of the diffusion approximation for holes in the n-region at the edge of the space-charge layer in a general p^+-n junction as follows.
   (a) Show that the ratio of the relevant drift to diffusion current densities of holes is = EL_p/V_t where E is the electric field, L_p is the hole diffusion length and V_t is the thermal voltage.
   (b) Assuming the electron current density to be uniform in the space-charge layer, and to be predominantly due to diffusion at the space-charge layer edge on the p-side but due to drift at the space-charge layer edge on the n-side, show that the electric field is given by $E = (V_t/L_n)(n_p/n_{n0})$.
   (c) Using the results of (a) and (b), show that the ratio of the hole drift to diffusion current densities is < p_n / n_{n0}, which is the injection level on the n-side, and so, << 1 under the approximations of the ideal diode model.

8) A Silicon diode forward biased at a fixed current is being used as a thermometer. The diode voltage is 0.62 V at 300 K. (a) How much will this voltage change when the temperature is varied by ±2 %. (b) Estimate the diode voltage at 50°C. Comment on the utility of the diode as a thermometer from these calculations.

Lec 24, 25: P-N Junction under reverse bias and small-signal conditions

9) A symmetrical abrupt Germanium p-n junction has an impurity concentration of 10^{15} cm^{-3} on both sides. Calculate the avalanche breakdown voltage if the maximum electric field at breakdown is 250 kV cm^{-1}. Calculate the breakdown voltage if the impurity concentration on the n-side remains the same, but on the p-side it becomes 10^{19} cm^{-3}.

10) An abrupt silicon p-n junction at 300 K has an area of 1 mm^2. The measured junction capacitance C_j (μF) as a function of the reverse bias of magnitude V_R (V) is given by the relation $C_j^{-2} = 2 \times 10^8 (0.6 + V_R)$. Estimate the built-in voltage, and the doping levels on the two sides of the junction.

11) The depletion region capacitance of a GaAs p^+-n junction diode is measured as a function of the reverse bias, and the following data are obtained. Check if it is a uniformly doped abrupt junction diode.

V_R (V)	0	0.5	1.0	3.0	5.0
C_j (pf)	19.9	17.3	15.6	11.6	9.8

Lec 26, 27: BJT evolution, device structure and transistor action

12) Trace the evolution of the BJT from the idea of a solid state triode.

13) Sketch the following for a typical modern small-signal bipolar junction transistor *to scale*: (a) cross-section and top view of the device structure; (b) DC I_C - V_{CE} curve for four different base currents. Mention whether the transistor is n-p-n or p-n-p.

14) In a p-n-p BJT, the emitter-base junction is forward biased by connecting a current source between the emitter and base, and the collector is shorted to base. Explain the transistor action by drawing the excess Carrier profiles in base and emitter, and discussing the variation of various current flow components, as the base width is reduced from very large to very small values compared to diffusion length in the base.

15) Sketch J_n, J_p and J as a function of distance from emitter to collector in a p-n-p BJT, wherein the emitter junction is forward biased and the collector junction is (a) shorted, and (b) reverse biased (with respect to the base).

Lec. 28-31: BJT – DC Model

16) The base region of a silicon n^+ p n^+ power transistor has a width of 100 μm, a minority carrier lifetime of 10 μs and a doping of 5 x 10^{14} cm^{-3}. Calculate the β of this device when the reverse bias across the collector-base junction is (a) 0 V and (b) 300 V. Note that, in this device, the collector junction depletion width is entirely on the base side of the junction.

17) Consider a p-n-p transistor operating in the active region at room temperature. Explain based on device physics, how the base current I_B will decrease and eventually change direction, as the temperature is increased gradually keeping the collector current I_C constant.

18) Consider a p-n-p transistor in which we have $N_E >> N_B >> N_C$ and negligible recombination in the base. The device is operating with a base current I_B and an emitter to collector voltage V_{EC}.
   (a) Derive expressions for the following voltages in terms of I_B and physical parameters, namely – doping levels, lifetimes and diffusion coefficients in various regions, and base width: (i) V_{EB} when $V_{EC} = 0$; (ii) V_{EC} when $I_C = 0$.
   (b) Calculate the voltages in (a) for I_B = 100 μA and the following parameter values: emitter- N_E = 5 x 10^{17} cm^{-3}, τ_E = 0.1 μs; base - N_B = 1 x 10^{16} cm^{-3}, W_B = 1 μm; collector - N_C = 1 x 10^{15} cm^{-3}, τ_C = 10 μs; A = 1 mm^2. W_B is between the depletion edges in the base and independent of bias conditions.

Lec. 32: BJT – Small-signal model

19) What are the typical values of the components of a common-emitter *h*-parameter equivalent circuit and a hybrid-π equivalent circuit of a bipolar junction transistor ?

20) How will you determine the parameters h_{fe} and h_{oe} from a family of I_C-V_{CE} characteristics?

Lec 33-35: MOS junction under DC conditions

21) A MOS junction has a p-type substrate, a positive fixed charge, $\phi_{ms} = 0$ and $V_T < 0$. Sketch its space-charge, electric field and potential distributions from gate to substrate, under zero gate to bulk bias.

22) For the junction in (21), sketch the band diagram from gate to substrate, under zero gate to bulk bias.

23) An Aluminum gate MOS capacitor is fabricated on an n-silicon substrate with $N_d = 10^{15}$ cm^{-3}, $t_{ox} = 0.12$ μm and $Q_f/q = 3 \times 10^{11}$ cm^{-2}. (a) Estimate V_{FB} and the electric field in the oxide at threshold. (b) Sketch the energy band diagram from gate to substrate at the onset of inversion to scale, showing the critical values on the diagram.

24) A 0.5 μm thick gate oxide is grown on a uniformly doped n-silicon sample with $N_d = 1.5 \times 10^{15}$ cm^{-3}. Assuming the oxide to be charge free, calculate the surface potential and the gate voltage for making the surface intrinsic.

Lec 36,37: MOS junction under small-signal conditions and body effect

25) High frequency capacitance measurements of a two terminal Aluminum gate MOS junction yielded the following results: maximum capacitance occurring for large negative gate voltage is 18 nF-cm^{-2}, minimum capacitance occurring for large positive gate voltage is 70% of the maximum capacitance, $V_T = 2$ V. Determine the following: (a) oxide thickness; (b) polarity and concentration of doping in the substrate; (c) flat-band voltage; (d) fixed charge concentration.

26) A p-channel MOSFET has $t_{ox} = 0.1$ μm, $Q_f/q = 8 \times 10^{10}$ cm^{-2} $N_d = 1.5 \times 10^{16}$ cm^{-3} and the gate is heavily doped with boron. Calculate the bulk to source bias required to get $V_T = -2.7$ V.

Lec 38: MOSFET – Evolution, device structure and characteristics to be modeled

27) Trace the evolution of the MOSFET from the discovery of the BJT.

28) Sketch the following for a typical modern small-signal MOSFET *to scale*: (a) cross-section and top view of the device structure; (b) DC $I_D - V_{DS}$ curve for four different gate biases.

Lec 39-41: MOSFET – DC and small-signal models

29) An Aluminum gate enhancement type n-channel MOSFET has $N_a = 6 \times 10^{15}$ cm^{-3}, $t_{ox} = 0.1$ μm, $Q_f/q = 1 \times 10^{10}$ cm^{-2}, $W/L = 100$, $\mu_n = 500$ cm^{2}V^{-1}s^{-1}, $L = 10$ μm. (a) When the transistor is in the linear region with $V_{DS} = 0.5$ V, calculate the V_{GS} to obtain a drain current of 2 mA. Take $V_{BS} = 0$. (b) Estimate g_d, and g_m in (a). (c) Estimate I_D and g_m in saturation assuming the value of V_{GS} obtained in (a). (d) What changes will occur in the characteristics of the MOSFET when the gate metal is replaced by *p*-poly silicon doped with $N_a > 1 \times 10^{19}$ cm^{-3} operated at the same current in the linear region with $V_{DS} = 0.5$ V?

Lec 42: JFETs, MESFETs, HFETs, Solar Cells

30) Sketch simple schematics of a JFET, a MESFET, a HFET and a Solar Cell, and explain the operation of these devices briefly.